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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
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EXAMINER	
SOWARD, IDA M	

ART UNIT	PAPER NUMBER
2822	

DATE MAILED: 10/06/2004

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	09/844,347	ZENG, JUN	
	Examiner	Art Unit	
	Ida M Soward	2822	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *19 July 2004*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *23-29 and 31-39* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *23-29 and 32-39* is/are rejected.

7)☒ Claim(s) *23, 29, 31-32, 35-36 and 39* is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

This Office Action is in response to the Applicant's amendment filed July 19, 2004.

Claim Objections

The objection to claims 23, 32 and 36 has been withdrawn due to the amendment filed.

NEW Claim Objections

Claim 23, 29, 31-32, 35-36 and 39 are objected to because of the following informalities:

1. In claim 23, "**the**" should have been **said** in lines 3, 5, 9 and 15.
2. In claim 29, "**the**" should have been **said** in line 2 (twice).
3. Claim 31 depends on cancelled claim 30.
4. In claim 32, "**the**" should have been **said** in lines 3-5 on page 3 and line 7 on page 4.
5. In claim 35, "**the**" should have been **said** in line 3.
6. In claim 36, "**outwardly extending dielectric layer having sidewalls aligned with sidewalls of the trench**" is stated in lines 4-6 and lines 16-17. Appropriate correction is required.
7. Also, in claim 36, "**the**" should have been **said** in line 3 on page 4 and lines 1, 3-4, 6, 12 and 17 on page 5.
8. In claim 39, "**the**" should have been **said** in line 1 on page 6.

Appropriate correction is required.

Claim Rejections - 35 USC § 112

The rejection of claims 23, 32 and 36 under 35 U.S.C. 112, second paragraph, has been withdrawn due to the amendment filed.

Claim Rejections - 35 USC § 103

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 103 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which the subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

Claims 23-28, 32-34 and 36-38 are rejected under 35 U.S.C. 103(a) as being unpatentable over Kocon et al. (US 6,187,105, B1) in view of Williams et al. (US 2002/0019099 A1).

In regard to claim 23, Kocon et al. teach a MOSFET comprising: a semiconductor layer 103 having a trench therein; a gate conducting layer 205 in a lower portion of the trench; a dielectric layer 207; source regions 201 adjacent the dielectric layer 207; and source/body contact regions 210 laterally spaced apart from the trench and being recessed within the semiconductor layer 103 and non-interruptively contacting the source regions 201; the dielectric layer 207 extending outwardly from the semiconductor layer 103 the source regions 201 and the source/body contact regions 210 (Figure 31, col. 4, lines 45-63).

In regard to claim 24, Kocon et al. teach a source electrode 212 on the source regions 201 and on the dielectric layer 207 (Figure 31, col. 4, lines 45-63).

In regard to claims 26 and 33, Kocon et al. teach a portion of the source regions 201 including a recess over the source/body contact regions 210 (Figure 30, col. 4, lines 45-63).

In regard to claim 27, Kocon et al. teach a portion of the source regions 201 including an opening exposing the source/body contact regions 210; and further comprising a source electrode 212 on the source regions 201, on the dielectric layer 207, and on the source/body contact regions 210 (Figure 30, col. 4, lines 45-63).

In regard to claims 28, 34 and 38, 0.0 to 1 micron fail in the range of equal to or less than about 1 micron, outwardly extending dielectric layer 207 clearly extends from the source regions 201 greater than zero (Figure 31).

In regard to claim 32, Kocon et al. teach a MOSFET comprising: a semiconductor layer 103 having a trench therein; a gate dielectric layer lining 204 in the trench; a gate conducting layer 205 in a lower portion of the trench; a dielectric layer 207; source regions 201 adjacent the dielectric layer 207; source/body contact regions 210 laterally spaced from the gate conducting layer 205 and non-interruptively contacting the source regions 201; the dielectric layer 207 extending outwardly from the semiconductor layer 103, the source regions 201 and the source/body contact regions 210; a source electrode 212 on the source regions 201 and on the dielectric layer 207; and at least one conductive via between the source electrode 212 and the source/body contact regions 210 and extending through the source regions 201 (Figures 29-30, col. 4, lines 45-63).

In regard to claim 36, Kocon et al. teach a MOSFET comprising: a semiconductor layer 103 having a trench therein; a gate dielectric layer 204 lining the trench; a gate conducting layer 205 in a lower portion of the trench; a dielectric layer 207 extending outwardly from the semiconductor layer 103; source regions 201 adjacent the dielectric layer 207 and including an opening therein; and source/body contact regions 210 laterally spaced from the gate conducting

layer 205 and non-interruptively contacting the source regions 201, the source/body contact regions 210 being exposed by the opening in the source regions 201; the dielectric layer 207 extending outwardly from the semiconductor layer 103, the source regions 201 and the source/body contact regions 210.

In regard to claim 37, Kocon et al. teach a source electrode 212 on the source regions 201, on the dielectric layer 207, and on the source/body contact regions 210 (Figures 30-31, col. 4, lines 45-63).

However, Kocon et al. fail to teach an outwardly extending dielectric layer having sidewalls aligned with sidewalls of the trench and in an upper portion of the trench.

Williams et al. teach an outwardly extending dielectric layer 116 having sidewalls aligned with sidewalls of the trench and in an upper portion of the trench (Figures 11E and 15D, pages 8-9, paragraphs [0118]-[0122], respectively).

Since Kocon et al. and Williams et al. are from the same field of endeavor (MOSFET devices with a semiconductor layer having a trench therein; a gate conducting layer in a lower portion of the trench; a dielectric layer in an upper portion of the trench; source regions adjacent the dielectric layer ; and source/body contact regions laterally spaced apart from the trench and being recessed within the semiconductor layer and non-interruptively contacting the source regions; the dielectric layer extending outwardly from the semiconductor layer the source regions and the source/body contact regions), the purpose disclosed by Williams et al. would have been recognized in the pertinent art of Kocon et al.

Therefore, it would have been obvious to one having ordinary skill in the art at the time the invention was made to modify the MOSFET structure as taught by Kocon et al. with the

MOSFET structure having an outwardly extending dielectric layer having sidewalls aligned with sidewalls of the trench and in an upper portion of the trench as taught by Williams et al. to protect the gate from subsequent processes (page 7, paragraph [0106]).

Claims 29, 35 and 39 are rejected under 35 U.S.C. 103(a) as being unpatentable over Kocon et al. (US 6,187,105, B1) and Williams et al. (US 2002/0019099 A1) as applied to claim 23-28, 32-34 and 36-38 above, and further in view of Mo et al. (US 6,710,406 B2).

Kocon et al. and Williams et al. teach all mentioned in the rejections above. However, Kocon et al. and Williams et al. fail to teach a gate conducting layer recessed in the trench within a range of 0.2 to 0.8 microns from the opening thereof.

Mo et al. teach a gate conducting layer 28 recessed in the trench 14 within a range of 0 to 0.4 microns, which is in the range of 0.2 to 0.8 microns (Figures 1A-1B, col. 4, lines 64-67).

Since Kocon et al., Williams et al. and Mo et al. are from the same field of endeavor (MOSFET devices with a semiconductor layer having a trench therein; a gate conducting layer in a lower portion of the trench; a dielectric layer in an upper portion of the trench; source regions adjacent the dielectric layer ; and source/body contact regions laterally spaced apart from the trench and being recessed within the semiconductor layer and non-interruptively contacting the source regions; the dielectric layer extending outwardly from the semiconductor layer the source regions and the source/body contact regions), the purpose disclosed by Mo et al. would have been pertinent in the art of Kocon et al. and Williams et al.

Therefore, it would have been obvious to one having ordinary skill in the ad at the time the invention was made to modify the MOSFET device structure of Williams et al. and the

MOSFET structure having an outwardly extending dielectric layer having sidewalls aligned with sidewalls of the trench and in an upper portion of the trench as taught by Williams et al. with the MOSFET structure having a gate recess depth as taught by Mo et al. to provide a device with excellent reliability (col. 2, lines 11-19).

Response to Arguments

Applicant's arguments with respect to claims 23-29 have been considered but are moot in view of the new ground(s) of rejection.

Conclusion

The prior art made of record and not relied upon is considered pertinent to applicant's disclosure.

The following patents are cited to further show the state of the art with respect to trenched MOSFETs:

Beasom (US 6,368,920 B1) Brush et al. (US 6,373,098 B1)

Floyd et al. (US 6,444,527 B1) Hshieh (US 6,262,453 B1).

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Ida M Soward whose telephone number is 571-272-1845. The examiner can normally be reached on Monday - Thursday, 6:30 am to 5:00 pm.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Amir Zarabian can be reached on 571-272-1852. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

IMS
September 29, 2004

AMIR ZARABIAN
SUPERVISORY PATENT EXAMINER
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